ABSTRACT OF THE DISCLOSURE

[22] Ultra narrow and thin polycrystalline silicon gate electrodes are formed by patterning a polysilicon gate precursor, reducing its width and height by selectively oxidizing its upper and side surfaces, and then removing the oxidized surfaces. Embodiments include patterning the polysilicon gate precursor with an oxide layer thereunder, ion implanting to form deep source/drain regions, forming a nitride layer on the substrate surface on each side of the polysilicon gate precursor, thermally oxidizing the upper and side surfaces of the polysilicon gate precursor thereby consuming silicon, and then removing the oxidized upper and side surfaces leaving a polysilicon gate electrode with a reduced width and a reduced height. Subsequent processing includes forming shallow source/drain extensions, forming dielectric sidewall spacers on the polysilicon gate electrode and then forming metal silicide layers on the upper surface of the polysilicon gate electrode and over the source/drain regions.